Ministry of Electronics & IT

Union Minister Shri Ashwini Vaishnaw interacts with Semiconductor Chip Design Companies approved under the DLI Scheme

Target of enabling at least 50 fabless semiconductor companies in next phase

Focus on six key semiconductor design domains: Compute Systems, RF, Networking, Power Management, Sensors and Memory

Government to Institute Deep Tech Awards in 2026

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Union Minister for Electronics and Information Technology Shri Ashwini Vaishnaw, interacted with **semiconductor chip design companies** approved under the **Design Linked Incentive (DLI) Scheme** of the **Semicon India Programme** in New Delhi today. The interaction focused on **reviewing progress**, **understanding design innovations**, and reinforcing the Government's commitment to building a robust, indigenous semiconductor design ecosystem. The DLI Scheme aims to accelerate domestic chip design capabilities by supporting startups and companies across areas such as SoCs, telecom, power management, AI, and IoT, thereby strengthening India's self-reliance in critical semiconductor technologies.

The DLI-supported companies are engaged in semiconductor design across a broad range of areas, including indigenous SoCs and ASICs for surveillance, networking and embedded systems, RISC-V–based processors and accelerators, and AI-enabled, low-power chips for IoT and edge applications. Their work also covers telecom and wireless chipsets, power management and mixed-signal ICs, and strategic sectors such as automotive, energy, space and defence, contributing to the development of a self-reliant semiconductor design ecosystem in the country. Advanced EDA tools have been provided to these organizations, leading to approximately 2.25 crore tool-hours of usage, with 67,000 students and over 1,000 startup engineers actively engaged. In academia, 122 designs have been taped out, with 56 chips fabricated at 180 nm at SCL, Mohali, while startups have completed 16 tape-outs, resulting in six chips fabricated at advanced foundry nodes as advance as 12 nm. Additionally, 75 patents have been filed by academic institutions and 10 patents by startups.

Addressing the stakeholders, Shri Vaishnaw said that the government's multi-year, ecosystem-driven approach to semiconductor development is delivering tangible results. He added that the programme was conceived in 2022 with a clear vision articulated by Prime Minister Narendra Modi, to build the entire semiconductor ecosystem, pursue a long-term strategy rather than isolated schemes, and transform India from a services-led economy into a product nation.

Highlighting the success of the **Design Linked Incentive (DLI) Scheme**, the Minister noted that while expectations were modest initially, the programme today supports **24 startups**, many of which have already completed tape-outs, validated products and found market traction. This, he said, has

validated the government's core approach of removing key barriers faced by semiconductor startups by providing access to advanced design tools, IP libraries, wafer and tape-out support—an architecture of support that is unique globally.

The Minister underlined that the comprehensive support extended by the India Semiconductor Mission to semiconductor startups is unparalleled, and the government now intends to **scale up the programme**, with a target of enabling at least **50 fabless semiconductor companies** in the country in the next phase. He expressed confidence that India would, in the coming years, see the emergence of globally competitive fabless companies comparable to leading international players.

Sharing feedback from recent global engagements at the **World Economic Forum in Davos**, the Minister said that international industry leaders have increasingly recognised the seriousness, scale and execution capability of India's semiconductor programme. From initial scepticism in 2022, global perception has shifted significantly, with industry leaders now keen to partner with India's growing semiconductor ecosystem.

The Minister outlined a focused strategy to strengthen India's semiconductor design capabilities across **six key system categories** - compute, RF and wireless, networking, power management, sensors, and memory. These categories, he said, form the foundational building blocks for most modern electronic systems and would enable India to design and build solutions for a wide range of applications spanning defence, space, automotive, railways, drones and other strategic sectors.

Referring to infrastructure development, the Minister stated that **SCL Mohali** will support tape-outs in the **180-nanometre range**, while advanced nodes up to **28 nanometres** will be enabled through the upcoming fabrication facility at **Dholera**, providing a strong manufacturing base to complement domestic design capabilities. He also highlighted the government's sustained focus on talent development, noting that against a target of 85,000 skilled professionals over ten years, over **67,000 semiconductor professionals have already been trained in just four years**.

Expressing confidence in India's growing role in the global semiconductor ecosystem, the Minister said that a significant share of the world's semiconductor design work would be carried out in India in the coming years, driven by domestic startups, engineers and innovators creating their own IP, patents and enterprises.

Looking ahead, the Minister said that by **2029**, India would achieve the capability to design and manufacture chips required for nearly **70–75 per cent of domestic applications**. Building on this foundation, the next phase under **Semicon 2.0** will focus on advanced manufacturing, with a clearly defined roadmap to achieve **3-nanometre and 2-nanometre technology nodes**. By **2035**, India aims to be among the **top semiconductor nations globally**.

The Minister further noted that startups supported under the scheme have attracted nearly **₹430 crore in venture capital funding**, reflecting growing confidence in India's design ecosystem. He informed that of the **24 startups** participating in the DLI programme, **14 startups have secured venture capital funding**. He said the India Semiconductor Mission, launched four years ago, has delivered strong outcomes, including **10 projects under construction**, **four projects expected to begin production this year**, and 67,000 students trained in semiconductor chip design across **315 academic institutions**.

The Minister also announced that the government will institute **Deep Tech Awards** in **2026** to recognise and encourage innovation across key sectors including semiconductors, artificial intelligence, biotechnology, space and other deep-tech domains. The first round of awards is expected to be held towards the end of the year.

During the event, several startups unveiled their tape-out milestones and commercialization roadmaps, enabled by funding and EDA tools support under the DLI Scheme. These startups highlighted the importance of indigenization at the component and chip level to achieve a trusted supply chain and self-reliance. They attributed their achievements to the effective enablement provided under the DLI Scheme. The event was also attended by the Secretary, MeitY, Shri S. Krishnan, and CEO, ISM, Shri Amitesh Kumar Sinha.

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